UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/472,869	12/28/1999	Tae-Yong Sohn	Q57124	9316

7590 01/09/2002

SUGHRUE MION ZINN
MACPEAK & SEAS PLLC
2100 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 200373202

EXAMINER
NATNAEL, PAULOS M

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 01/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/472,869	SOHN, TAE-YONG	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) ____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

2. Claim **10** is rejected under 35 U.S.C. 102(e) as being anticipated by Han et al., U.S. Pat. No. 6,297,850..

Considering claim **10**, Han et al. discloses all claimed subject matter, note;

a) the claimed method of receiving said input broadcast signal into said digital signal receiver is met by Image Processor 600 (FIG.2), which receives DTV image signal from video decoder 800. (Col. 4, 41-45)

B) the claimed method of detecting a frame rate of the input broadcast signal received is met by frame rate detector 100, which detects "a frame rate of an input digital image signal." (Col.3, lines 63-64)

c) the claimed method of selecting a clock frequency that corresponds to the frame rate which is detected is met by clock selector 320 (FIG.2), which selectively outputs either a clock signal of

74.25 MHZ or 74.175 MHZ according to an output signal of the OR gate 310. (Col. 4, lines 13-18)

d) the claimed method of outputting the clock frequency which is selected to components of the digital signal receiver that use the clock frequency to decode and display said input broadcast signal is met by "a clock generator **300** generating an appropriate clock signal according to the output signals of the frame detector 100 and the display mode detector 200..."(col. 3, lines 66 to col. 4, line 2) which clock signal is output to the image processor 600 as well as to the sync signal generator 500 and sync signal compensation unit 400. (See FIG.2)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim **1** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hwang, U.S. Pat. No. 6,097,437.

Considering claim **1**, Hwang discloses the following claimed subject matter, note;

a) the claimed first phase locked loop is met by W-PLL and Time Generator 30 FIG. 3,

b) the claimed second phase locked loop is by R-PLL and Time Generator 30 FIG. 3,

d) the claimed a controller for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of an input digital signal is met by microcomputer 20, (FIG.3). (Col. 4, lines 50-55)

Except for;

c) the claimed **switching portion for selecting a clock frequency** from one of the first and second phase locked loops according to a predetermined control signal;

Regarding c), Hwang does not specifically disclose a switching portion in Fig.3. However, Hwang discloses a multiplexer (FIG.1) that is clearly used to selectively switch the input signals of First AD converting section 202 and second AD converting section 207. Hwang also discloses the microcomputer 20 receives "the horizontal and vertical sync signals H-sync and V-sync from the host 10, determining a video mode, and generating data that indicates the number of dots per a period of the horizontal output signal according to the determined video mode. (Col. 4, lines 50-55) Therefore, it would have been obvious to the skilled in the art at the time the invention was made to readily recognize the teachings of Hwang and modify the reference of Hwang by adding a multiplexer or a switch to selectively switch the output of the two PLL circuit to the format converter 60, under the control of the microcomputer 20.

5. Claims **2-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hwang**, U.S. Pat. No. 6,097,437 in view of **Han** et al., U.S. Pat. No. 6,297,850.

Considering claim **2**, the claimed wherein the first phase locked loop generates a clock frequency of 74.25 MHZ, and wherein the second phase locked loop generates a clock frequency of 74.175 MHZ.

Regarding claim 2, Hwang doesn't specifically disclose the clock frequency outputted from the two PLL circuits. However, the two clock signals would have two different frequencies. Hans for example specifies two clock frequencies -- a 74.25 MHZ and another 74.175 as claimed -- selectively outputted from the clock generator 300 One of 74.25 MHZ and the other 74.175 as claimed. Therefore, it would have been obvious to the skilled in the art at the time the invention was made to readily recognize the teachings of the Han and modify the reference of Hwang to provide two clock frequency

Considering claim **3,** the claimed wherein the input digital signal has a frame rate selected from the group consisting of 60 Hz, 59.94 Hz, 30 Hz, 29.97 Hz, 24 H z and 23.97 H z, wherein if the frame rate of the input digital signal is one of 60 Hz, 30 Hz and 24 Hz, the controller controls the switching portion to select and output the clock frequency of the first phase locked loop, and wherein if the frame rate of the input digital signal is one of 59.94 Hz, 29.97 Hz and 23.97 Hz, the controller controls the switching portion to select the clock frequency from the second phase locked loop.

Regarding claim 3, Hwang doesn't specifically disclose frame rates. However, it is well known in the art that video frame rates such 60 Hz, 59.94 Hz, 30 Hz, 29.97 Hz, 24 H z and 23.97

H z are used. For example, Han discloses that the frame rate detector 100 detects either a format of 60 Hz, 30 Hz, 24 H z or 59.94 Hz, 30 Hz, 29.97 Hz, or 29.98 H z, and accordingly sends a signal to the clock generator to output either a clock frequency of 74.25 or 74.175 MHZ. Therefore, it would have been obvious for those skilled in the art at the time the invention was made to readily recognize the teachings of Han and modify the reference of Hwang to provide frame rates for the PLLs.

Considering claim **4**, the claimed wherein the first phase locked loop generates a clock frequency of 74.25 MHZ, and wherein the second phase locked loop generates a clock frequency of 74.175 MHZ.

Regarding **4,** see rejection of claim **2.**

6. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Han et al., U.S. Pat. No. 6,297,850.

Considering claim **5**, Han discloses the following claimed subject matter, note;

a) the claimed video decoder for decoding a video component of a received digital signal into a first input digital signal is met by video decoder 800 (FIG.2), which outputs the DTV image signal. (Col. 4, lines 41-50)

c) the claimed a format converter for receiving either of said first and second input digital signals, according to which of said first and second input digital signals is present, said format converter for converting the input digital signal received by said format converter into a predetermined display format output signal is met by image processor 600 (FIG.2).

D) the claimed controller for detecting a frame rate of the input digital signal received by said format converter and outputting a timing control signal corresponding to the frame rate detected is met by frame rate detector 100, which detects "a frame rate of an input digital image signal." (Col.3, lines 63-64)

E) the claimed clock frequency providing means for providing a clock frequency according to the timing control signal output by said controller, said clock frequency provided to the format converter for converting the input digital signal received by said format converter into said predetermined display output signal; said clock frequency also provided to said video decoder when said second input digital signal is not present at said format converter is met by clock generator 300, (FIG.2) which generates "an appropriate clock signal according to the output signals of the frame detector 100 and the display mode detector 200..."(col. 3, lines 66 to col. 4, line 2) which clock signal is output to the image processor 600 as well as to the sync signal generator 500 and sync signal compensation unit 400.

Except for;

b) the claimed an analog to digital converter for converting a received analog video signal into a second input digital signal;

Regarding b), Han does not specifically disclose an analog to digital converter, however, Examiner takes official Notice in that the analog to digital converter (A/D) is well known in the art and would have been obvious to the skill in the art at the time the invention was made to provide an A/D converter to convert the received NTSC analog image signal into a second input digital signal in the image processor.

7. Claim **6-9 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Han** et al., U.S. Pat. No. 6,297,850 in view of **Hwang**, U.S. Pat. No. 6,097,437.

Considering claim **6**, Han discloses the following claimed subject matter, note;

c) the claimed switching portion that receivers said timing control signal from said controller and said switching portion outputting one of said first and second clock frequencies corresponding to the received timing control signal as said clock frequency is met by the clock selector 320, (FIG.2) which selectively outputs either a clock signal of 74.25 MHZ or a clock signal of 74.175 MHZ according to an output signal of the OR gate 310;

Except for;

a) the claimed first phase locked loop for generating a first clock.

b) the claimed first phase locked loop for generating a second clock.

Regarding a) and b), Han doesn't specifically disclose PLL. However, Han discloses a clock generator 300 that generates two different types of clock and selectively outputs one of them. Hwang discloses two PLL and time generators 30 and 40 which generate a read clock signal R-CLK and a write clock signal W-CLK. Therefore, it would have been obvious to the skilled in the art at the time the invention was made to readily recognize the teaching of the prior art and modify the reference of Han to generate first and second clocks.

Considering claim **7,** the claimed on-screen graphics mixer for mixing desired graphics with said predetermined display format output signal to output a mixed graphics video signal, wherein said on-screen graphics mixer operates responsive to the clock frequency provided by said clock frequency providing means.

Regarding claim 7, Han doesn't specifically disclose on-screen display or a mixer. However, Examiner is taking Official Notice in that the on-screen displays and mixers are well known in the art and therefore would have been obvious to the skilled in the art at the time the invention was made to readily recognize the teaching of the prior art and modify the reference of Han to provide an on-screen graphics mixer.

Considering claim **8**, the claimed video signal processor for processing the mixed graphics video signal output form said on-screen graphics mixer is met by image processor 600.

Considering claim **9**, the claimed audio signal processing means for processing audio signals received in said digital signal receiver;

Regarding claim **9**, Han doesn't specifically disclose audio signal processing means. However, Examiner is taking Official Notice in that an audio signal processor is well known in the art and therefore would have been obvious to the skilled in the art at the time the invention was made to readily recognize the teaching of the prior art and modify the reference of Han to provide an audio signal processor.

Considering claim **11,** Han discloses the following claimed subject matter, note;

a) the claimed outputting a control signal from a controller is met by the input to display mode detector form I^{a}C or controller.

b) the claimed said control signal depending upon the frame rate which is detected is met by the frame rate detector 100;

c) the claimed receiving said control signal into a selector is met by the input to gate 310;

Except for;

d) the claiemd said selector connected to outputs of a plurality of phase locked loops, wherein each phase locked loop has a predetermined clock frequency, selecting one predetermined clock frequency of one of said plurality of phase locked loops based upon the control signal received by the selector;

Regarding d), see rejection of claim 6 (a) and (b).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reitmeier, U.S. Pat. No. 6,118,486 discloses synchronous multiple format video processing method and apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Paulos Natnael** whose telephone number is **(703) 305-0019.** The examiner can normally be reached on **Monday through Thursday** from **8:00 a. M.** to **5:00 p.m.** The examiner can also be reached on alternate **Fridays.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **John Miller,** can be reached on **(703)305-4795.**

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is **(703)305-3900.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications intended for entry)

or:

(703)872-9314 (for informal or draft communications, please label "PROPOSED" OR "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, V.A. Sixth Floor (Receptionist).

Paulos M. Natnael PMN

December 30, 2001

JOHN W. MILLER
PATENT EXAMINER